ABSTRACT OF THE DISCLOSURE

Digital delay locked loops which generate fixed angle delayed (e.g., quadrature) clock signals based on a reference clock signal and that accounts for clock signal delay. The number of quadrature delay elements is calculated based on the number of delay elements needed to provide one or more cycles of delay, and adjusted to reflect system clock delay. The digital delay locked loop also acquires a locked state quickly by sampling more frequently before acquiring the lock than after. Furthermore, jitter is reduced by introducing hysteresis into the sampling process, and by disabling the delay element adjustment process during jitter sensitive times. Lock stability is improved by introducing hysteresis into the lock detection process.

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